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Docket No. XA-9377
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TO THE ASSISTANT COMMISSIONER FOR PATENTS
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Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

POWER AMPLIFIER MODULE

and invented by:

Kiichi Yamashita
Tomonori Tanoue
Shizuo Kondo

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having 37 pages and including the following:
   a. ☒ Descriptive Title of the Invention
   b. ☐ Cross References to Related Applications *(if applicable)*
   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   d. ☐ Reference to Microfiche Appendix *(if applicable)*
   e. ☒ Background of the Invention
   f. ☒ Brief Summary of the Invention
   g. ☒ Brief Description of the Drawings *(if drawings filed)*
   h. ☒ Detailed Description
   i. ☒ Claim(s) as Classified Below
   j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 8
   b. ☐ Informal Number of Sheets _____
4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Computer Program in Microfiche *(Appendix)*
7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*
9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*
10. ☐ English Translation Document *(if applicable)*
11. ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
12. ☐ Preliminary Amendment
13. ☒ Acknowledgment postcard
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Accompanying Application Parts (Continued)

15. ☒ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

Japanese Application No. 11-306266 filed October 28, 1999 (TO FOLLOW)

16. ☒ Additional Enclosures *(please identify below):*

Letter Proposing Drawing Changes

Request That Application Not Be Published Pursuant To 35 U.S.C. 122(b)(2)

17. ☐ Pursuant to 35 U.S.C. 122(b)(2), Applicant hereby requests that this patent application not be published pursuant to 35 U.S.C. 122(b)(1). Applicant hereby certifies that the invention disclosed in this application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication of applications 18 months after filing of the application.

Warning

An applicant who makes a request not to publish, but who subsequently files in a foreign country or under a multilateral international agreement specified in 35 U.S.C. 122(b)(2)(B)(i), must notify the Director of such filing not later than 45 days after the date of the filing of such foreign or international application. A failure of the applicant to provide such notice within the prescribed period shall result in the application being regarded as abandoned, unless it is shown to the satisfaction of the Director that the delay in submitting the notice was unintentional.

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Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	14	- 20 =	0	x	$18.00	$0.00
Indep. Claims	1	- 3 =	0	x	$80.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$710.00
OTHER FEE *(specify purpose)*		**Assignment Recordation Fee**				$40.00
					TOTAL FILING FEE	$750.00

☒ A check in the amount of **$750.00** to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **22-0585** as described below. A duplicate copy of this sheet is enclosed.

- ☐ Charge the amount of as filing fee.
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- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Mitchell W. Shapiro
Signature

Dated: **October 20, 2000**

Reg. No. 31,568

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cc:

SPECIFICATION

TITLE OF THE INVENTION

POWER AMPLIFIER MODULE

FIELD OF THE INVENTION

The present invention relates to a power amplifier module, particularly to a technology that is effectively applied to a power amplifier module for a cellular phone system with the capability of output power control to be used on portable terminal equipment used in a mobile communication system.

BACKGROUND OF THE INVENTION

Significant growth has lately been found in the market of cellular phone systems, typically, such as a Global System for Mobile Communication (GSM) and a Personal Communication Network (PCN) and this tendency is anticipated to continue in the future. One of the requirements of such systems as GSM and PCN is that the output power of portable terminal equipment can be controlled, dependent on the distance from a base station to the equipment. This can be fulfilled by controlling the gain of the power amplifier module installed on the equipment.

Fig. 9 shows an example of a typical conventionally used power amplifier module with three stages of output power control. In this power amplifier module, a signal input through a pin 062 is amplified by first-stage, second-stage, third-stage amplifiers 601, 602, 603, and output through a pin 064. Power source voltage is applied to a pin 063. At this time, an output power control circuit 607 controls the gains of the amplifiers 601, 602, and 603 by changing an idling current that determines a DC bias of transistors 604, 605, and 606. Hetero-Bipolar Transistors (GaAsHBTs) are used as the transistors 604, 605, and 606.

Using the above third-stage amplifier 603 and its output power control circuit 607, the output power control function will be explained below. The amplifier 603 comprises a transistor 606, a resistor 611, coupling capacitance 612, and an output adjustment circuit 613. The output power control circuit 607 comprises transistors 608, 609, and 610 and resistors 614, 615, and 616. Here, the diode-connected transistors 609 and 610 and the diode-connected transistors 608 and 606 form a current mirror circuit. Current that is as large as mirror ratio times the current flowing across the transistors 609 and 610 flows through the transistor 606 as the idling current.

The voltage across the transistors 609 and 610 becomes substantially constant when an output power control

voltage applied to a pin 061 becomes higher than the boot voltage of these transistors. In the voltage region higher than the boot voltage, the idling current increases or decreases in proportion to the control voltage. Because the gain depends on this idling current, the gain can be made variable by controlling the idling current. In fact, the output power control uses this characteristic. In the conventional module example shown in Fig. 9, the idling current to flow in the first-stage amplifier 601 is generated by applying a voltage produced by diving the control voltage by resistance to the base of the amplifier. This means taken is different from the means of idling current supply for the second-stage amplifier 602 and the third-stage amplifier 603.

SUMMARY OF THE INVENTION

Output power control characteristic requirements are that output power shall change as a monotone function relative to the control voltage in a wide dynamic range of 70 to 80 dB (the output power typically ranges between -40 and 35 dBm for GSM) and that its change factor, or in other words, control sensitivity shall fall within a predetermined value (which is, typically, 150 dB/V or below). In the conventional module example shown in Fig.

9, however, the idling current changes in proportion to the control voltage.

For the circuit shown in Fig. 9, control sensitivity $\partial P_{21}/\partial$ Vapc becomes greater as the signal level decreases. This is expressed as:

P_{21} = a constant + 20 logI_d (dB), I_d = (Vapc - 2 Vb)/Rapc (1)

$\partial P_{21}/\partial$ Vapc = 20/(Vapc - 2 Vb) (dB/V) (2)

where Vapc > 2 Vb

$\partial P_{21}/\partial$ Vapc = 0 where Vapc $\leqq$ 2 Vb (3)

The above equations (1) and (2), where P_{21} is gain, I_d is idling current, Vapc is control voltage, Vb is base-emitter voltage of the transistors 609 and 610, and Rapc is the resistance of the resistor 614, indicate the following. When the control voltage exceeds the sum of the boot voltages of the transistors 609 and 610, the idling current starts to flow, resulting in the greatest control sensitivity. The control sensitivity becomes theoretically infinity, but there are many cases where the input signal power level is actually 0 dBm or higher and the DC current generated by a self-bias effect causes the control sensitivity to be around 300 dB/V. For equation (3), idling current I_d is generated if Vapc $\leqq$ 2 Vb, but there is no input of the required control voltage Vapc, causing that $\partial P_{21}/\partial$ Vapc = 0.

For the above conventional module example, the first-stage amplifier 601, the second-stage amplifier 602, and the third-stage amplifier 603 operate in different states. Due to this, a kink is liable to take place in the control characteristic, which made it difficult to satisfy the output power control characteristic requirements of the power amplifier module. As apparent from a characteristic chart shown in Fig. 10, the control characteristic greatly changes, depending on the power at the input signal pin, and a control voltage Vapc level section representing extremely high sensitivity appears. When the sensitivity becomes extremely high as the characteristic chart shows, the output power Pout greatly changes with even small change of the control voltage Vapc. When a feedback to return such excessive change of the output power Pout to normal is applied, the characteristic also responds to the feedback and such a oscillation state appears that the output power Pout cyclically changes for a period corresponding to the feedback loop.

An object of the present invention is to provide a power amplifier module featuring that its output power characteristic smoothly changes as the input control voltage changes and that its control sensitivity is stable over a wide dynamic range. Another object of the present invention is to provide a power amplifier module of

convenient service. The above and other objects as well as noticeable features of the present invention would be elucidated from the whole text of the present specification and the related drawings.

A typical power amplifier module embodied by the invention disclosed herein will be summarized below. The power amplifier module accomplishes output power control in such a manner that: upon the reception of control input voltage, idling current is generated and adjusted such that it exponentially changes, relative to the control input voltage and the idling current is supplied to a power amplifier element.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent during the following discussion of the accompanying drawings, wherein:

Fig. 1 is a basic circuit diagram showing a power amplifier module as a preferred embodiment of the present invention;

Fig. 2 is a circuit diagram showing a power amplifier module as another preferred embodiment of the present invention;

Fig. 3 is a circuit diagram showing a concrete power amplifier module as another preferred embodiment of the present invention;

Fig. 4 is a circuit diagram showing another concrete power amplifier module as another preferred embodiment of the present invention;

Fig. 5 is a block diagram showing a power amplifier module of three-stage configuration as another preferred embodiment of the present invention;

Fig. 6 is a block diagram of a power amplifier module as another preferred embodiment of the present invention;

Fig.7 is a characteristic chart for explaining the operation of power amplifier modules that are embodiments of the present invention;

Fig. 8 is an overall block diagram of mobile communication equipment as a preferred embodiment on which a power amplifier module offered by the present invention is used;

Fig. 9 is a circuit diagram showing an example of prior art; and

Fig. 10 is a characteristic chart for explaining the operation of the power amplifier module shown in Fig. 9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows a basic circuit diagram of a power amplifier module as a preferred embodiment of the present invention. Any of the circuit elements in Fig. 1 is a discrete circuit module comprising a single semiconductor integrated circuit or a plurality of semiconductor integrated circuits and an external component connected to it or them. The power amplifier module of first embodiment comprises an amplifier 6 that consists of an output transistor 2, an adjustment circuit 4, and coupling capacitance 5 and an output power control circuit 1 that consists of a V-I logarithmic conversion circuit 11, a constant current source 7, input transistors 3 and 8, and an impedance circuit 9.

The V-I logarithmic conversion circuit 11 executes logarithmic conversion of an input control voltage that is input through a pin 03 into current. This circuit 11 enables that the idling current to flow in the output transistor 2 behaves to exponentially change, relative to the input control voltage. The transistor 8 takes the duty of supplying the DC component of a base current that is generated as an increment by the self-bias effect during large-signal operation mode and flows across the output transistor 2.

The impedance circuit 9 is used to prevent the instability of operation due to that a high-frequency signal

of the input signals input through the pin 01 flows through the above-mentioned input transistor 3. Reference number 04 is a power source pin. The input transistor 3 forms a current mirror circuit in conjunction with the output transistor 2 and has a current sensing function. Therefore, when a reference current from the constant current source 7 is allowed to flow across the input transistor 3, current that is as large as mirror ratio times the reference current is allowed to flow across the transistor 3 as the idling current.

In the above-mentioned conventional module example shown in Fig. 9, the idling current changes in proportion to the control voltage, whereas, as a feature of the circuitry of this first embodiment, the idling current is adjusted such that it exponentially changes, relative to the input control voltage. The following equations give gain P_{21} and control sensitivity $\partial P_{21}/\partial$ Vapc in small-signal operation mode of first embodiment:

$$P_{21} = \text{a constant} + \alpha \text{ Vapc/Vt} \times 20 \log e \text{ (dB)},$$

$$I_d = I_s \exp(\alpha \text{ Vapc}) \quad (4)$$

$$\partial P_{21}/\partial \text{ Vapc} = \alpha/\text{Vt} \times 20 \log e = 347\,\alpha \text{ (dB/V)} \quad (5)$$

where I_s and Vt (up to 25 mV) are physical constants and α is a coefficient. Equation (4) indicates that the gain is proportional to the input control voltage Vapc. From

this, as is indicated in equation (5), it is seen that control sensitivity is constant in the present invention and desired control sensitivity can be obtained if coefficient α is set at a suitable value. For example, set coefficient α at 0.5 or less in order to give control sensitivity of 150 dB/V or below. This is attributed to the adjusted behavior of the idling current I_d that exponentially changes, relative to the input control voltage Vapc. Most power amplifier modules used for practical application consist of a plurality of amplifiers. In practical situations, it is advisable to suitably allot the desired control sensitivity required for a power amplifier module among the multiple stages of amplifiers, according to their capabilities.

In the present invention, the relation of exponential function between the current supplied from the constant current source 7 and the input control voltage Vapc holds true. Thus, the idling current I_d exponentially changes, relative to the input control voltage Vapc, as was indicated in equation (4). Here, the value of the idling current I_d is determined from such DC bias of the output transistor 2 as to give desired output power and efficiency. On the other hand, an input signal is input through a pin 01, passes through the coupling capacitance 5, and after being amplified through the output transistor 2 and the adjustment circuit 4, it is output through a pin 02. Because

the idling current I_d exponentially changes, relative to the input control voltage Vapc, the gain (dB), or in other words, output power (dBm) increases or decreases in proportion to the input control voltage Vapc.

Therefore, constant control sensitivity such as a value of 347α (dB/V) for an input control voltage Vapc, as was indicated in equation (5), can be obtained. During the operation explained above, a smooth output power control characteristic with little kinks can be measured as apparent from the characteristic chart shown in Fig. 7. Here, even if the power at the input signal pin is variable among decibel values -4 dBm, 0 dBm, 4 dBm, and 6 dBm, stable output power control can be achieved. In this way, the invention can provide a power amplifier module with an exceedingly good control characteristic and of convenient service.

For the transistors 2, 3, and 8, any type of bipolar transistors such as GaAsHBTs, SiGeHBTs, or Si bipolar transistors can be applicable, as will be described later. Because the transistors 2 and 3 form a current mirror circuit, it is desirable that they are same type transistors and integrated on a same chip. For a current supply circuit 10 that supplies current to the transistors 2 and 3, an integrated circuit to which Si bipolar process is applied as well as HBT may be used. The V-I logarithmic conversion circuit 11 and the constant current source 7 may be any

circuit type, provided they function, assuring that the reference current flows across the transistor 3, while changing exponentially, relative to the control voltage.

Fig. 2 shows a circuit diagram of a power amplifier module as another preferred embodiment of the present invention. This second embodiment module comprises three stages of power amplifiers connected in tandem. This configuration of the power amplifier module may comprise two stages for systems of relatively small output power requirement, for example, such as a Code Division Multiple Access (CDMA) system.

Unlike the above-mentioned conventional multi-stage amplifier module shown in Fig. 9, three stages of amplifiers of second embodiment are supplied with the reference current that determines the idling current to flow through the transistors in the stages from an output power control circuit 101 that executes control operation by same means. The idling currents flowing across transistors 105, 106, and 107 for amplification (corresponding to the above-mentioned transistor 2) in amplifiers 102, 103, and 104 are as large as mirror ratio times the currents flowing across current sensing transistors 108, 109, and 110 (corresponding to the above-mentioned input transistor 3), respectively.

Note that different current mirror ratios are set for the amplifiers 102, 103, and 104, according to the difference in the dimensions of the transistors 105 and 108, the transistors 106 and 109, and the transistors 107 and 110. The smallest mirror ratio is set for the first-stage transistor 105 for which the smallest operating power is required. The greatest mirror ratio is set for the last-stage transistor 107 for which the greatest operating power is required. The greater the mirror ratio, the greater the idling current flows through the transistor.

According to the second embodiment, the transistors 105, 106, and 107 carry different idling currents that are determined by different current mirror ratios as described above, and consequently the amplifiers fundamentally operate in the same manner even if input power levels are different. Therefore, the amplifier module can be embodied, exhibiting the smoother output power control characteristic apparent from the characteristic chart shown in Fig. 7, as compared with the conventional module example where the first-stage amplifier and the second-stage and third-stage amplifiers operate in different manners. In fact, the output power characteristic of the combined amplifiers of second embodiment exhibits smooth linear change with little kinks, which is made possible by the present invention.

Then, the circuit operation of second embodiment will be explained below. An input signal is applied to a pin 011 of the power amplifier module. The input signal passes through an adjustment circuit 111 where the signal source impedance is adjusted to an impedance match for input to the transistor 105 and is conveyed to the transistor 105 where its power is amplified. The amplified signal passes through an adjustment circuit 112 where the output impedance of the transistor 105 is adjusted to an impedance match for input to the transistor 106 and is supplied to the base of the transistor 106.

The signal thus conveyed to the transistor 106 is similarly conveyed from the transistor 106 through an adjustment circuit 113 to the transistor 197 and passes through an adjustment circuit 114, during which its power is serially amplified, and eventually it is output through a pin 012. As described above, a constant value of control sensitivity is given for a control voltage. If the amplifiers 102, 103, and 104 respectively have control sensitivity $\partial P_{21}/\partial$ Vapc, control sensitivity $\partial P'_{21}/\partial$ Vapc, and control sensitivity $\partial P''_{21}/\partial$ Vapc, the control sensitivity of the whole power amplifier module $\partial P_{021}/\partial$ Vapc is given by:

$$\partial P_{021}/\partial \text{Vapc} = \partial P_{21}/\partial \text{Vapc} + \partial P'_{21}/\partial \text{Vapc} + \partial P''_{21}/\partial \text{Vapc} \quad (6)$$

The result is the sum of the values of control sensitivity of all amplifiers stages.

Equation (6) indicates that desired control sensitivity of the module is obtained by assigning required sensitivity components to the stages of amplifiers and the percentages of the components are optional. If desired control sensitivity is, for example, 150 dB/V or below and its even components are assigned to the amplifier stages, assign control sensitivity of 50 dB/V or below to each stage of amplifier so that the intention can be met.

A current supply circuit 115 or the amplifiers and the output power control circuit may be integrated on a single chip by applying Si bipolar transistors and SiGeHBT process. It is desirable to integrate the transistors 105 through 110 on a same chip in order to reduce the size of the power amplifier module as well as provide uniform characteristics.

Fig. 3 shows a circuit diagram of a concrete power amplifier module as another preferred embodiment of the present invention. An output power control circuit 350 is to establish the relation of exponential function between the idling current and the control voltage such that the idling current exponentially changes, relative to the control voltage. For this purpose, it is advisable to make the reference current behave as the exponential function of

the control voltage when flowing across an input transistor 316 that forms a current mirror circuit in conjunction with an output transistor 317.

The method and circuit operation for embodying this will be described below. First, a V-I conversion circuit 351 generates current that is proportional to the input control voltage Vapc that is input through a pin 013. When the input control voltage Vapc exceeds the base-emitter voltage of a transistor 302, the current determined by a resistor 301 starts to flow through the transistor 302. Because the transistors 302 and a transistor 303 form a current mirror circuit, current that is as large as mirror ratio times the current flowing through the transistor 302 then starts to flow across the transistor 303.

After a current mirror circuit formed by transistors 304 and 308 reverses the direction of the current, the current is supplied via a transistor 309 to a resistor 307 and converted into voltage again. At this time, a transistor 305 supplies current to a transistor 306, thereby forming a pseudo voltage source. Voltage to be generated in the resistor 307 changes from the origin voltage that is generated by the above pseudo voltage source, that is, the base-emitter voltage of the transistor 306. The above process is carried out as preparation for establishing the relation of exponential function between

the reference current to flow across a transistor 316 and the input control voltage Vapc. Meanwhile, because the voltage occurring across the resistor 307 is proportional to the input control voltage Vapc, a value of the α coefficient in the equations (4) and (5) can be determined by using the ratio of the resistance of the resistor 307 to the resistance of the resistor 301, which eventually can determine control sensitivity.

For example, increasing the resistance of the resistor 307 causes control sensitivity to increase because the voltage across the resistor 307 rises; inversely, decreasing the resistance causes control sensitivity to decrease. This means that control sensitivity can be determined by properly selecting a value of the α coefficient. The α coefficient primarily depends on the relative ratio of the resistance of the resistor 307 to the resistance of the resistor 301. Thus, the value of α is substantially constant, regardless of the productive deviation of the resistors. In other words, the control circuit of third embodiment has control sensitivity that is not susceptible to productive deviation, provided its circuit elements are packaged on a single semiconductor integrated circuit.

The voltage occurred across the resistor 307 is conducted via level-shift transistors 309 and 311 to the

base of a transistor 312 where it is converted into a collector current of the transistor 312. At this time, because the emitter of the transistor 312 is grounded, the collector current is caused to exponentially change, according to the relation of exponential function between the current and the base voltage, that is, input control voltage Vapc.

After its direction is reversed by a current mirror circuit formed by transistors 313 and 314, that is, a constant current source, this collector current is supplied to the transistor 316 as reference current. A temperature characteristic control circuit 353 performs the task of adjusting the temperature characteristic of the reference current flowing through the transistor 316. Because the base-emitter voltage of the transistor 317 has a negative coefficient of temperature, the collector current continues to increase as temperature rises. The temperature characteristic control circuit 353 sets the temperature characteristic of the reference current to be supplied to the transistor 316 so that the coefficient of temperature of the current at high temperature will be less than the coefficient of temperature of the current at normal temperature. In this way, the circuit 353 functions to suppress the increase of the current due to the rise of the temperature of the transistor 317.

A transistor 315 supplies the DC component increment of the current to flow in the base of the transistor 317 when an amplifier 356 operates in large-signal mode. The output power control circuit 350 can be integrated by the Si process. However, the transistor 316 and the transistor 317 are same devices and should be integrated on a same chip.

Fig. 4 shows a circuit diagram of another concrete power amplifier module as another preferred embodiment of the present invention. This circuit of fourth embodiment has an additional output limit function. To the collector of a transistor 312 where the idling current is generated that exponentially changes as described above, a resistor 318 is connected. Voltage occurring across the resistor 318 is applied to the base-emitter of a transistor 319. The transistor 319 performs output limit action by using its base-emitter voltage as a reference voltage for limiting. Specifically, when the voltage drop occurring as the output current from the transistor 312 flows across the above resistor 318 exceeds the base-emitter voltage of the above transistor 319, the transistor 319 is activated and forms a bypass path of the current from a power source pin 04 to the collector of the transistor 312. Consequently, even if the above input control voltage Vapc further increases, which in turn increases the control current generated in the

transistor 312, the increment of the current flows through the transistor 319. Therefore, the current to be supplied to the above transistor 313 is constant and the gain of the output transistor 317 is limited.

Fig. 5 shows a block diagram of a power amplifier module of three-stage configuration as another preferred embodiment of the present invention. An output power control circuit 501 that controls the idling current supply to an amplifier 510 may be configured such that the control circuit 350 in Fig. 3 or Fig. 4 and its duplicates, a total of three control circuits are used in tandem as presented in Fig. 2. In this fifth embodiment, however, for circuit simplification purposes, the circuit 501 is configured as follows. A V-I current conversion circuit 351, a circuit for setting of coefficient of I-V conversion 352, a temperature characteristic control circuit 353, and a V-I logarithmic conversion circuit 354 are common ones that are shared with three stages of amplification. Only a current supply circuit 355 is configured to have three stages for three stages of amplification in the amplifier 510, comprising three constant current sources, each of which consists of the transistors 313 and 314 in Fig. 3 or Fig. 4 and three DC supplies, each of which consists of the transistors 315 and 316 that supply DC current and idling current to the transistor 317. The basic operation of the

fifth embodiment module is the same as that of the embodiment shown in Fig. 2 and its explanation will not be repeated.

Fig. 6 shows a block diagram of a power amplifier module as another preferred embodiment of the present invention. In this sixth embodiment module, there are two duplicated systems of the output power control circuits 501 shown in Fig. 5 to operate for two different systems, for example, GSM and PCN systems. These output power control circuits 591 have a function of switching between amplifiers 511 and 512. The module includes circuits 502 and 504 for switching between both amplifiers by a Vcnt control signal that is input through a pin 052 and current limit circuits 503 and 505 for limiting a rapidly increasing reference current due to the rise of control voltage as described above with Fig. 4.

Switching between the amplifiers is performed in accordance with, for example, the following condition setting. When the Vcnt control signal is "High" level (lower than 2 V), the amplifier for GSM system is active and the other amplifier for PCN system is inactive. When the Vcnt control signal is "Low" level, inversely, the amplifier for GSM is inactive and the other amplifier for PCN is active. Alternatively, the above levels of the Vcnt control signal may be upside down.

The current limit circuits 503 and 505 in Fig. 6 can be embodied as follows. As shown in Fig. 4, the resistor 318 for current sensing is connected to the collector end of the transistor 312 and both ends of the resistor 318 are connected to the base-and-emitter-coupled transistor 319 for current bypassing. Because the voltage across the resistor 318 becomes substantially constant when it exceeds the base-emitter voltage of the bypassing transistor 319, further extra current is bypassed via the transistor 319. In this way, the above-mentioned current limit function can be implemented. The current limit level is determined by the resistor 318.

Fig. 8 shows an overall block diagram of mobile communication equipment as a preferred embodiment on which a power amplifier module offered by the present invention is used. A typical example of this mobile communication equipment is a portable mobile phone as mentioned above. Signals received by an antenna are amplified in a receive front end, converted into an intermediate frequency by a mixer, and conveyed through an intermediate signal processing circuit IF-IC to a tone processing circuit. A gain control signal periodically included among the above received signals is decoded in a microprocessor CPU, which is not limited to a specific one, where an input control

voltage to be supplied to a power amplifier (power amplifier module) is generated.

The power amplifier executes gain control in accordance with the above input control voltage and generates a send output signal. Part of the power loss is fed back to the above microprocessor CPU via a power coupler so that power control within a given range is performed as explained above. A frequency synthesizer generates an oscillating signal corresponding to the received signal frequency by using a reference oscillator TCXO, a voltage control oscillator VCO, and a PLL loop. This oscillating signal is conveyed to the mixer in the receive front end and supplied to a modulator as well. In the above tone processing circuit, the received signal drives a receiver from which a tone signal is output. Voice to send is converted into electric signals in a microphone and the signals are conveyed through the tone processing circuit and a modulator/demodulator to the modulator.

In such mobile communication equipment, the above power coupler is used or the power source current flowing in the power amplifier circuit is sensed to determine whether power output operation is performed within a given range as specified for send operation and a feedback signal is generated. By means of such feedback loop, the power amplifier executes gain control operation and this may cause

oscillation. This oscillation mechanism is as follows. If a partial range of control sensitivity to input control voltage is extremely high, the output power excessively changes when the corresponding input control voltage is supplied. Feedback action to return the excessive change to normal recurs at delay timing during a feedback loop and this causes the output power to fluctuate largely.

Because a maximum distance between base stations is 10 miles (about 16 km), permitted for the above-mentioned GSM system, the output of a portable mobile phone must be controlled on a level ranging between 13 dBm and 43 dBm in 2-dB steps. This output control always controls the send power output of the portable mobile phone. In fact, the output control operation must be performed in accordance with control signals periodically transmitted from a base station. The power amplifier module provided by the present invention has substantially constant control sensitivity for all the region of input control voltages. Its stable control sensitivity over a wide dynamic range enables mobile communication equipment such as the above portable mobile phone to execute high-quality signal transmission.

According to the present invention, as explained above, the idling current to flow the power amplifier module exponentially changes, relative to output power control signals. Thus, the invention enables proportional or linear

gain (dB) control in accordance with the input control voltage, providing required stable control sensitivity. As concerns a power amplifier module of multistage configuration, for example, two stages or three stages, because idling current supply to each amplifier stage for power control is performed by same means, the module can be designed to exhibit a good control characteristic with little kinks. Furthermore, the invention is beneficial for cost reduction because the output power control circuit can be fabricated with Si bipolar transistors and the power amplification stages may be fabricated with GaAsHBT, SiGe-HBT, and Si bipolar transistors in combination.

The forgoing embodiments produce the following effects:

(1) A power amplifier module accomplishes output power control in the following way: upon the reception of control input voltage, idling current is generated and adjusted such that it exponentially changes, relative to the control input voltage and the idling current is supplied to a power amplifier element. As the input control voltage changes, the output power characteristic smoothly changes. The power amplifier module features stable control sensitivity over a wide dynamic range.

(2) In addition, a control circuit for implementing the above control is configured with a circuit for converting

the input control voltage into current, a circuit for generating a reference voltage from the current into which the input control voltage has been converted and setting a gradient of voltage that changes in proportion to the input control voltage, and a circuit for converting the voltage into the idling current that exponentially changes. Thereby, required stable control sensitivity can be set

(3) In addition, the power amplifier module is configured with a plurality of stages of amplifiers connected in tandem and a plurality of control circuits that receive the control input voltage in common and separately supply the idling current to one of the stages of amplifiers. Because the amplifier stages operate in the same way, the power amplifier module can be designed to exhibit a good control characteristic with little kinks.

(4) In addition, the power amplifier module uses a common control circuit comprising the circuit for converting the input control voltage into current, the circuit for generating a reference voltage from the current into which the input control voltage has been converted and setting a gradient of voltage that changes in proportion to the input control voltage, and the circuit for converting the voltage into the idling current that exponentially changes. This eliminates the possibility of supply of varying idling currents which otherwise might occur among a plurality of

idling current generators. The power amplifier module further includes a plurality of circuits for supplying the idling current to the multiple stages of amplifiers such that each circuit serves each amplifier with the idling current. In this way, the entire module circuit can be designed to be simple.

(5) In addition, the amplifier is fabricated with GaAsHBTs packaged on a semiconductor integrated circuit including a pair of an input transistor and an output transistor; the input transistor carries the above idling current and forms a current mirror circuit in conjunction with the output transistor. The control circuit is fabricated with Si transistors or GaAsHBTs packaged on a semiconductor integrated circuit. Thereby, high-frequency power output operation required for portable mobile phones can be implemented.

(6) In addition, the amplifier is fabricated with SiGeHBTs or Si bipolar transistors packaged on a semiconductor integrated circuit including a pair of an input transistor and an output transistor; the input transistor carries the idling current and forms a current mirror circuit in conjunction with the output transistor. The control circuit is fabricated with SiGeHBTs or Si bipolar transistors. Thereby, high-frequency power output operation required for portable mobile phones can be implemented.

(7) In addition, the power amplifier module further includes a circuit for limiting the idling current when the input control voltage has reached a certain level. Thereby, the module can be designed to perform stable operation with low power consumption.

(8) In addition, the power amplifier further includes a circuit by which the temperature characteristic of the idling current can be set optionally. Thereby, stable power output operation not susceptible to ambient temperature can be achieved.

The present embodiments explained above are to be considered illustrative and the present invention is not limited to the foregoing embodiments. Of course, the invention may be embodied in other modification forms within a scope not departing from the spirit or essence thereof. For example, for the first embodiment shown in Fig. 1, the input transistor 3 that is used as a reference current sensing device is not limited to some transistor type. Instead, a diode or diode-connected transistors of the same material as the transistor 2 for amplification may be used. This substitution does not alter the relation of exponential function between the input control voltage and the idling current.

Mobile communication equipment to which the present invention is applied includes, in addition to those such as

mobile phones that perform tone or voice signal transmission/reception, those that perform digital signal transmission/reception to/from a personal computer or other similar mobile communication equipment via a digital telephone switch network by converting digital signals into signals in a tone signal frequency band. For such digital signal transmission/reception, the present invention makes the transmission signal level stable, which can achieve data communications at a higher rate. The present invention can be widely used for power amplifier modules used on such mobile communication equipment.

A typical implementation of the invention disclosed herein produces effects that will be summarized below. According to the present invention, idling current to flow a power amplifier exponentially changes, relative to output power control signals, so that gain can be controlled in proportion to the control voltage and required control sensitivity can be obtained. For a power amplifier module of two-stage or three-stage configuration, because idling current supply to each amplifier stage for power control can be performed by same means, the module can be designed to exhibit a good control characteristic with little kinks.

Although the invention has been described in its preferred form with a certain degree of particularity, it is understood that the present disclosure of the preferred

form has been changed in the details of construction and the combination and arrangement of parts may be resorted to without departing from the spirit and the scope of the invention as hereinafter claimed.

WHAT IS CLAIMED IS:

1. A power amplifier module comprising:

an amplifier; and

a control circuit for supplying the amplifier with an idling current that controls the output power of the amplifier,

wherein the control circuit receives input control voltage and makes the idling current behave so as to exponentially change, relative to the input control voltage.

2. The power amplifier module according to claim 1, wherein the control circuit including:

a circuit for converting the input control voltage into current;

a circuit for generating a reference voltage from the current into which the input control voltage has been converted and setting a gradient of voltage that changes in proportion to the input control voltage; and

a circuit for converting the voltage into the idling current that changes exponentially.

3. The power amplifier module according to claim 1, wherein the amplifier is a complex comprising a plurality

of stages of amplifiers connected in tandem, and wherein the control circuit is a complex comprising a plurality of circuits that receive the control input voltage in common and separately supply the idling current to one of the plurality of stages of amplifiers.

4. The power amplifier module according to claim 3, wherein a common circuit is formed, comprising the circuit for converting the input control voltage into current, the circuit for generating a reference voltage from the current into which the input control voltage has been converted and setting a gradient of voltage that changes in proportion to the input control voltage, and the circuit for converting the voltage into the idling current that changes exponentially, and

wherein a plurality of circuits are provided for supplying the idling current to the plurality of stages of amplifiers such that each circuit serves each stage of amplifier with the idling current.

5. The power amplifier module according to claim 1, wherein the amplifier is fabricated with GaAsHBTs packaged on a semiconductor integrated circuit including a pair of an input transistor and an output transistor, the input transistor carrying the idling current and forming a current

mirror circuit in conjunction with the output transistor, and

wherein the control circuit is fabricated with Si transistors or GaAsHBTs packaged on a semiconductor integrated circuit.

6. The power amplifier module according to claim 1,

wherein the amplifier is fabricated with SiGeHBTs or Si bipolar transistors packaged on a semiconductor integrated circuit including a pair of an input transistor and an output transistor, the input transistor carrying the idling current and forming a current mirror circuit in conjunction with the output transistor, and

wherein the control circuit is fabricated with SiGeHBTs or Si bipolar transistors packaged on a semiconductor integrated circuit.

7. The power amplifier module according to claim 1,

wherein the power amplifier module further includes a circuit for limiting the idling current once the input control voltage has reached a predetermined level.

8. The power amplifier module according to claim 1,

wherein the power amplifier module further includes a circuit by which the temperature characteristic of the idling current can be set optionally.

9. The power amplifier module according to claim 2,

wherein the amplifier is a complex comprising a plurality of stages of amplifiers connected in tandem, and

wherein the control circuit is a complex comprising a plurality of circuits that receive the control input voltage in common and separately supply the idling current to one of the plurality of stages of amplifiers.

10. The power amplifier module according to claim 9, wherein a common circuit is formed, comprising the circuit for converting the input control voltage into current, the circuit for generating a reference voltage from the current into which the input control voltage has been converted and setting a gradient of voltage that changes in proportion to the input control voltage, and the circuit for converting the voltage into the idling current that changes exponentially,

wherein a plurality of circuits are provided for supplying the idling current to the plurality of stages of amplifiers such that each circuit serves each stage of amplifier with the idling current.

11. The power amplifier module according to claim 2, wherein the amplifier is fabricated with GaAsHBTs packaged on a semiconductor integrated circuit including a pair of an input transistor and an output transistor, the input transistor carrying the idling current and forming a current mirror circuit in conjunction with the output transistor, and

wherein the control circuit is fabricated with Si transistors or GaAsHBTs packaged on a semiconductor integrated circuit.

12. The power amplifier module according to claim 2, wherein the amplifier is fabricated with SiGeHBTs or Si bipolar transistors packaged on a semiconductor integrated circuit including a pair of an input transistor and an output transistor, the input transistor carrying the idling current and forming a current mirror circuit in conjunction with the output transistor, and

wherein the control circuit is fabricated with SiGeHBTs or Si bipolar transistors packaged on a semiconductor integrated circuit.

13. The power amplifier module according to claim 3, wherein the power amplifier module further includes a

circuit for limiting the idling current once the input control voltage has reached a predetermined level.

14. The power amplifier module according to claim 2, wherein the power amplifier module further includes a circuit by which the temperature characteristic of the idling current can be set optionally.

ABSTRACT OF THE DISCLOSURE

The present invention provides a power amplifier module featuring that: its output power characteristic smoothly changes as the input control voltage changes; and its control sensitivity is stable over a wide dynamic range. By same means, idling current for gain setting is supplied to a single amplifier element or all of multiple stages of amplifier elements of the power amplifier module. By making this idling current behave so as to exponentially change, relative to input control voltage, the invention enables output power control proportional to the input control voltage.

FIG. 1

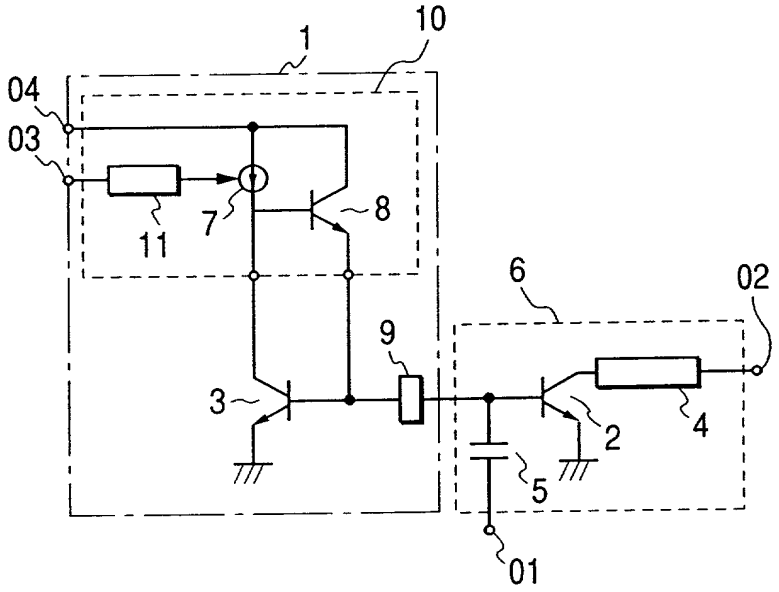


FIG. 2

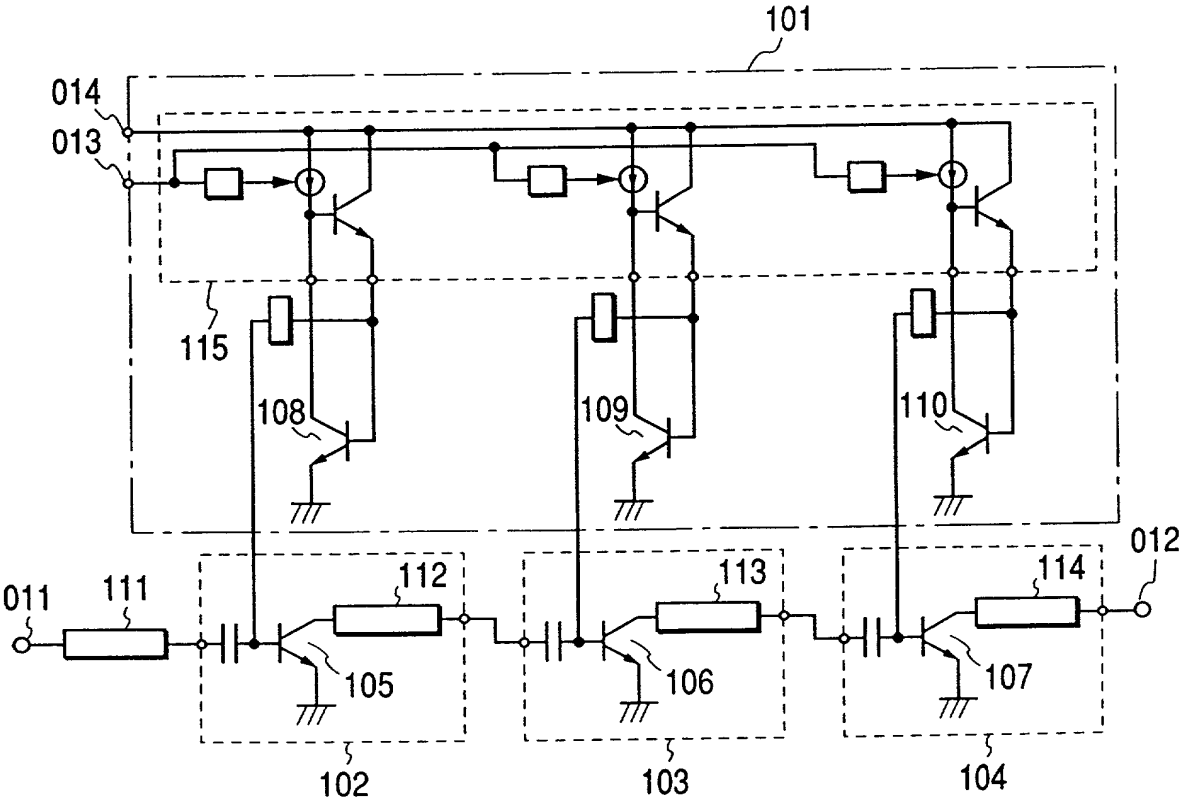


FIG. 3

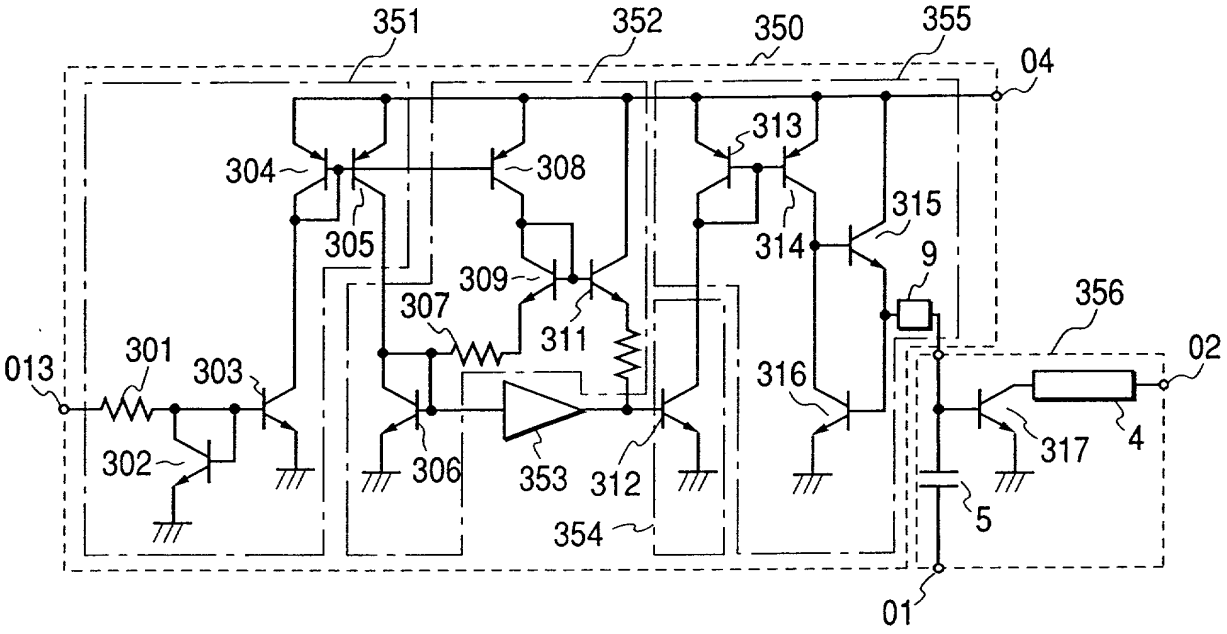


FIG. 4

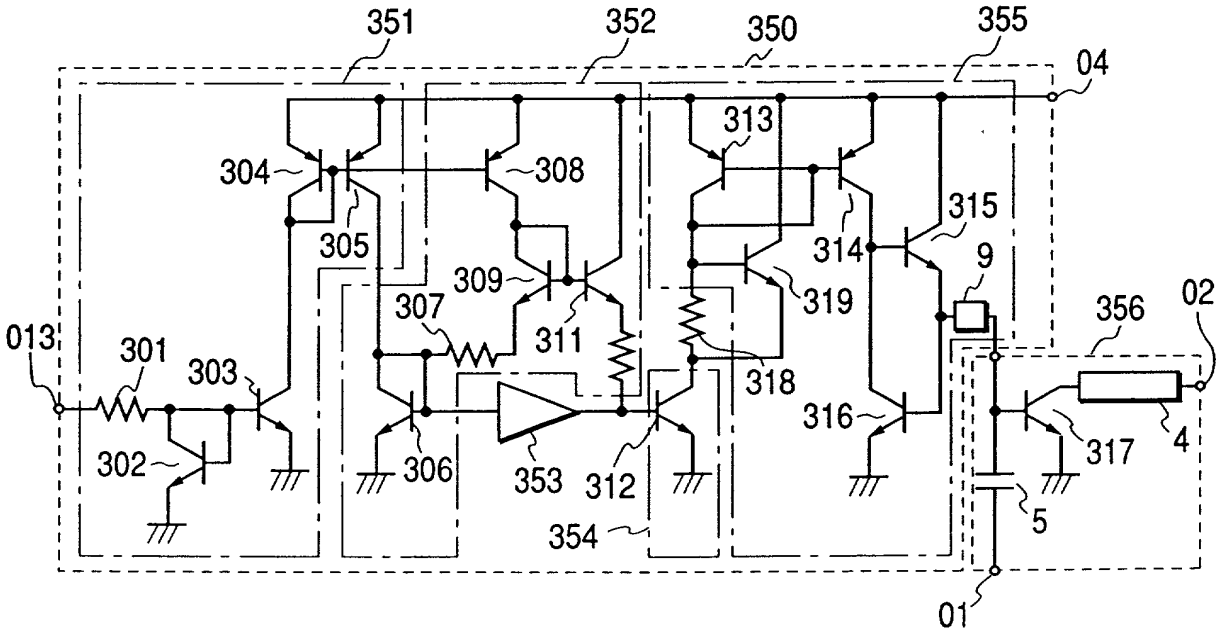
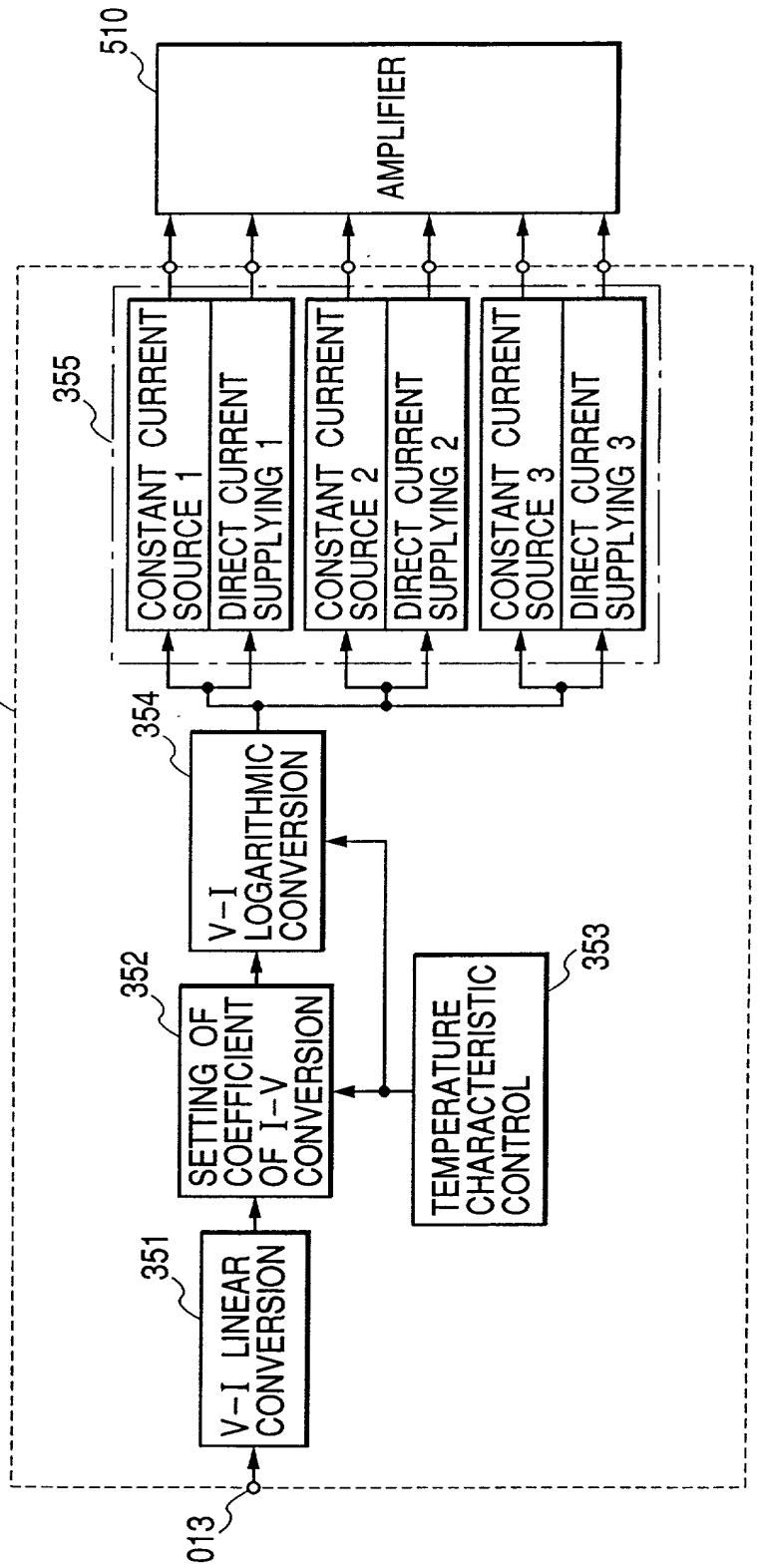


FIG. 5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CONSTANT CURRENT SOURCE 1
DIRECT CURRENT SUPPLYING 1
CONSTANT CURRENT SOURCE 2
DIRECT CURRENT SUPPLYING 2
CONSTANT CURRENT SOURCE 3
DIRECT CURRENT SUPPLYING 3
501
354
V–I LOGARITHMIC CONVERSION
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SETTING OF COEFFICIENT OF I–V CONVERSION
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TEMPERATURE CHARACTERISTIC CONTROL
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V–I LINEAR CONVERSION
013

FIG. 6

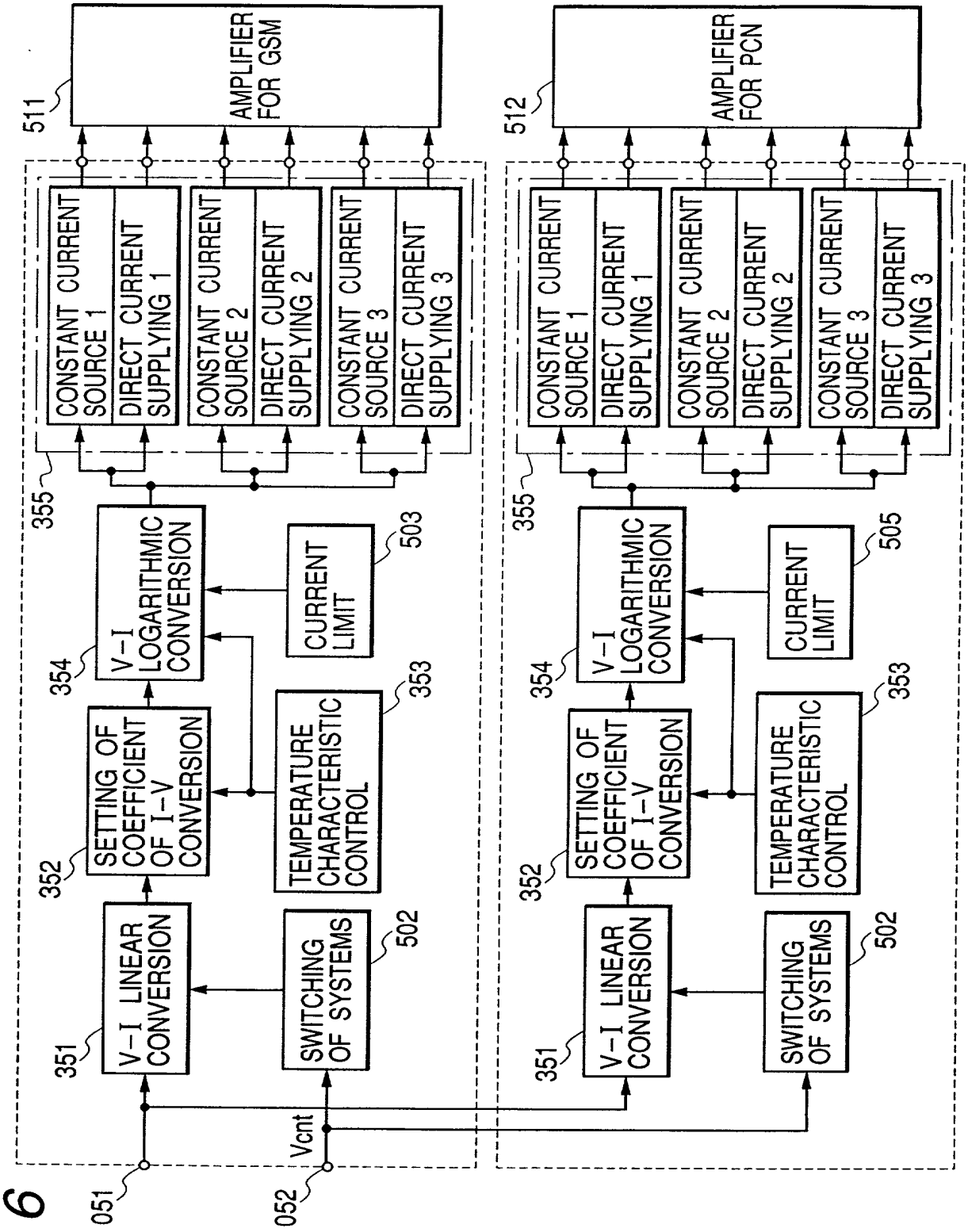

FIG. 7

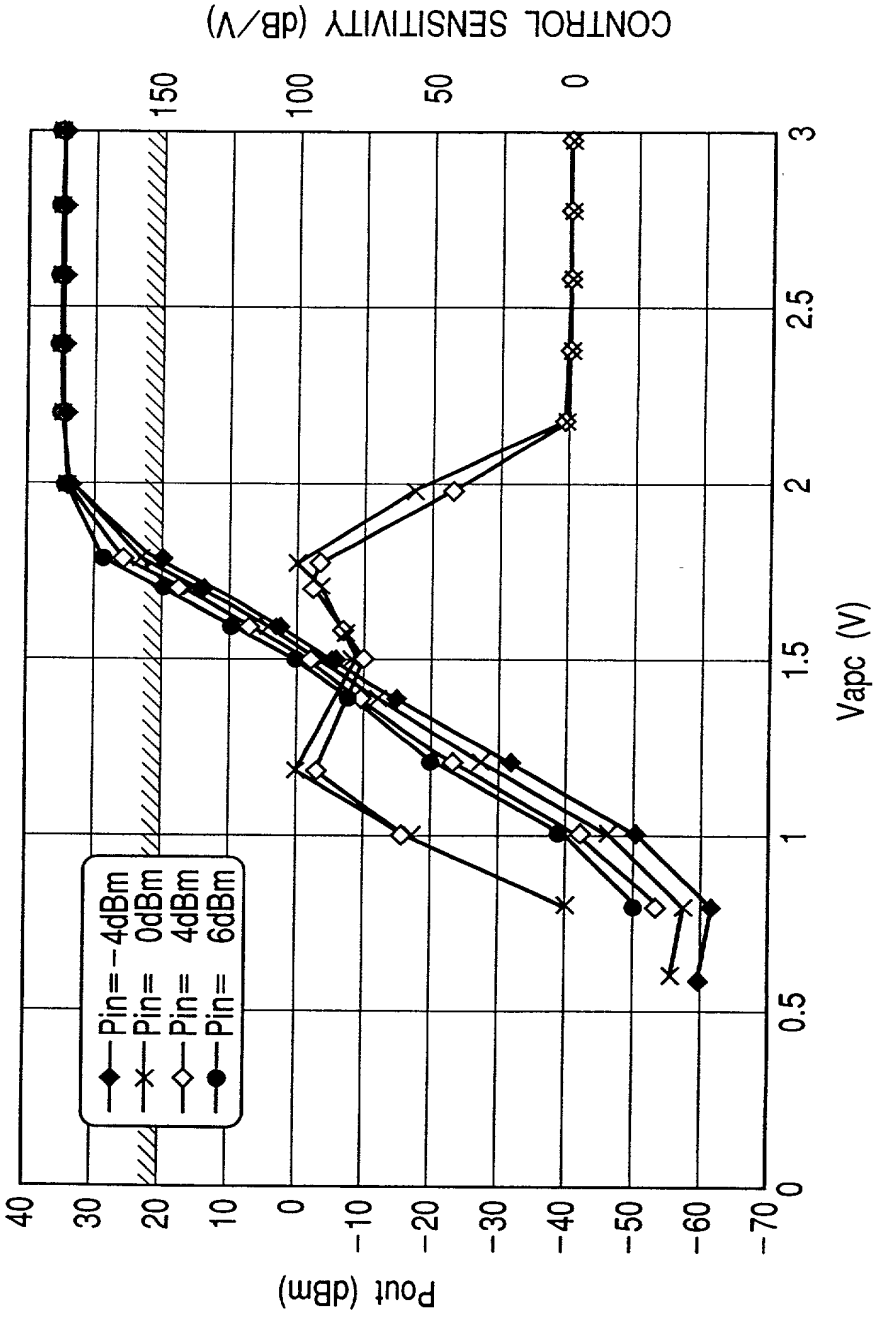

FIG. 8

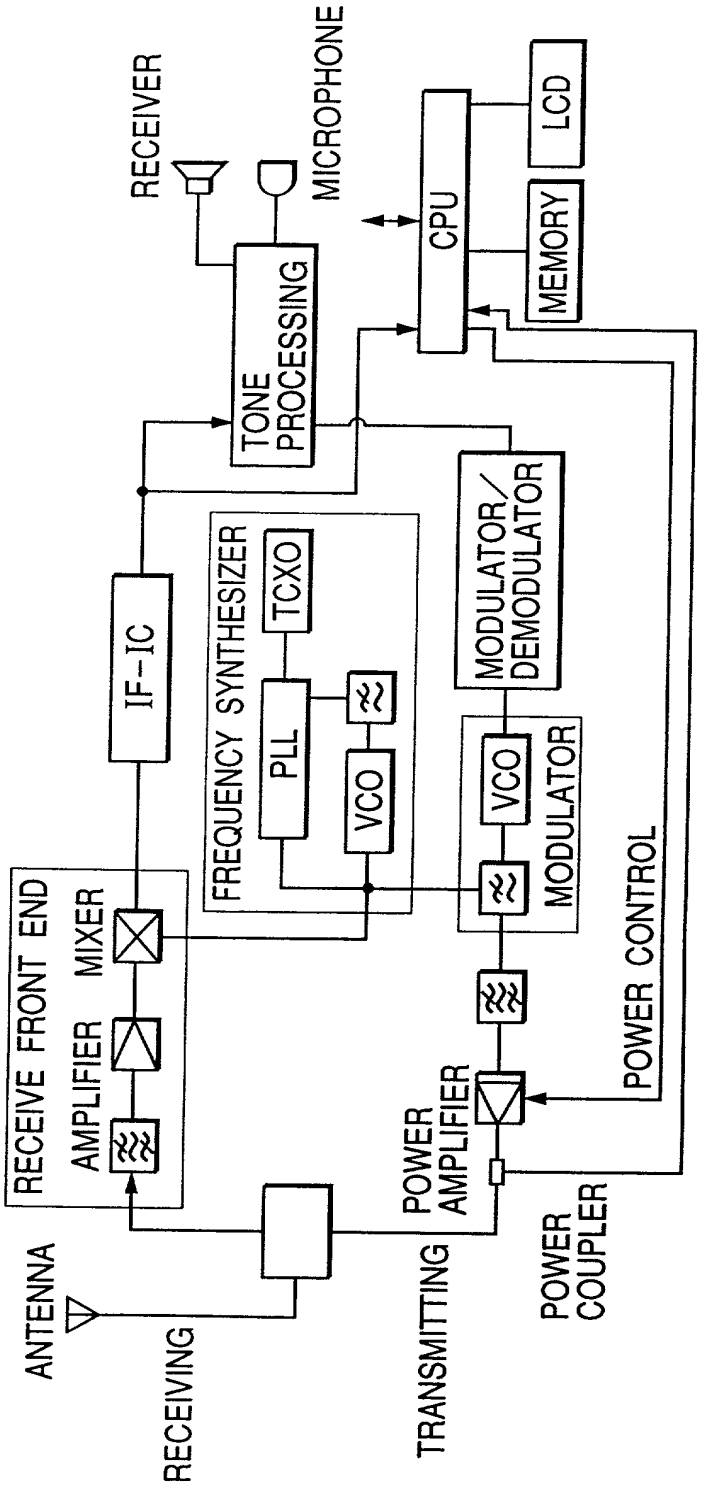
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FIG. 9

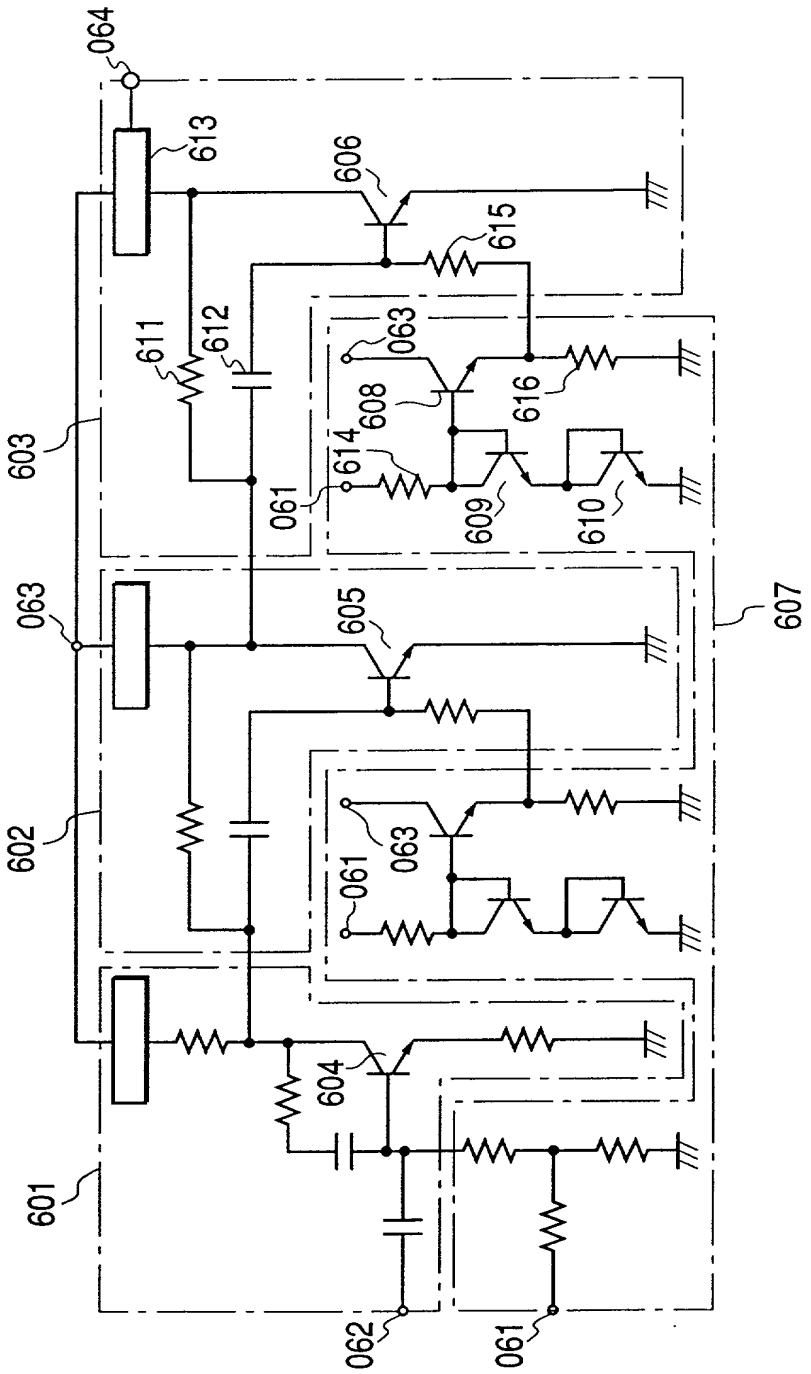
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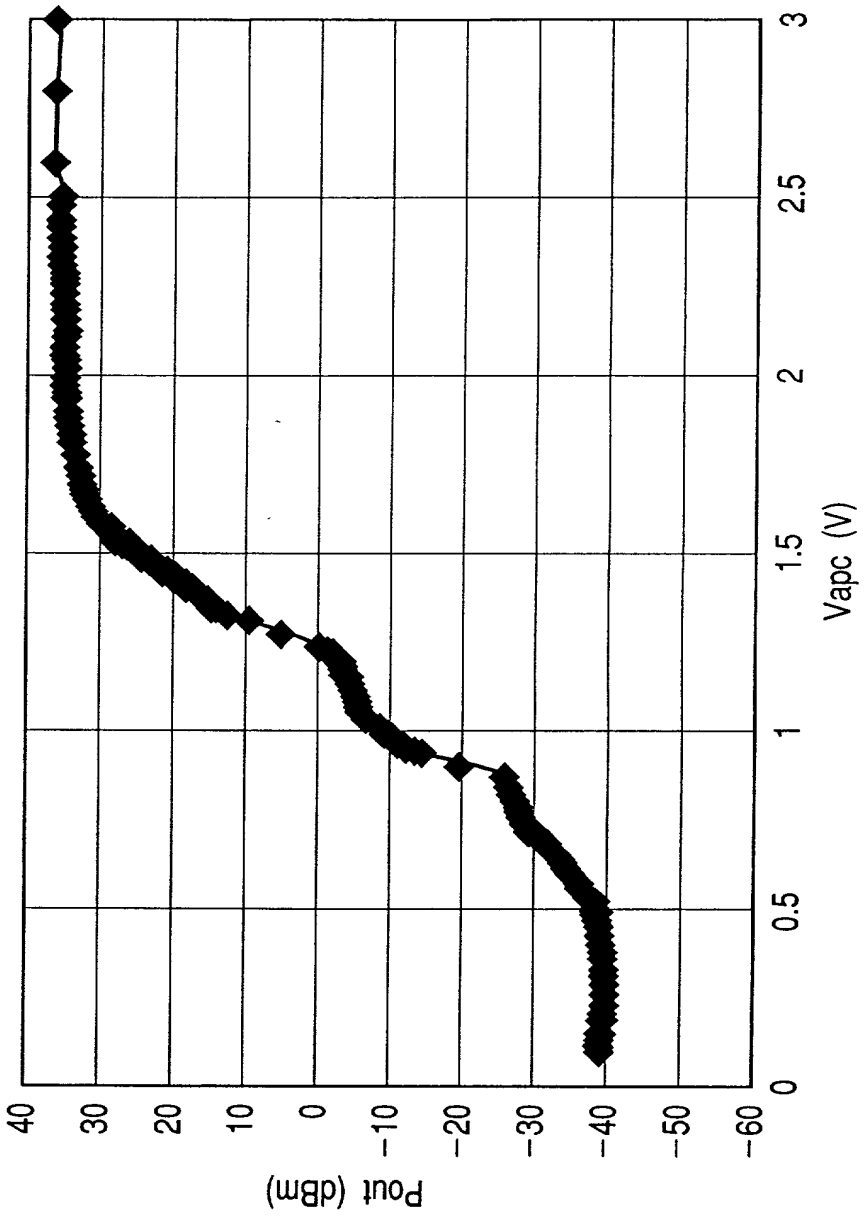
FIG. 10



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Declaration and Power of Attorney For Patent Application

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日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

POWER AMPLIFIER MODULE

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

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(該当する場合) _____に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条 (b) 項に基き下記の、 米国以外の国の少なくとも一カ国を指定している特許協力条約３６５ (a) 項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
11－306266	Japan	28／October／ 1999	☐
			☐

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I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c) に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*)

Nelson H. Shapiro, Reg. No. 17,095, Mitchell W. Shapiro, Reg. No. 31,568, and the other practitioners associated with the Customer Number 20,230

書類送付先

Send Correspondence to:
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直接電話連絡先： (名前及び電話番号)

Direct Telephone Calls to: (*name and telephone number*)
Telephone: (202) 467-8800
Fax: (202) 467-8900

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(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

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第二共同発明者の署名　日付	Second inventor's signature　Date Tomonori Tanoue　10/9/2000
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第三共同発明者の署名　日付	Third inventor's signature　Date Shizuo Kondo　10/9/2000
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国籍	Citizenship Japan
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第四共同発明者の署名　日付	Fourth inventor's signature　Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address
第五共同発明者名	Full name of fifth joint inventor, if any
第五共同発明者の署名　日付	Fifth inventor's signature　Date
住所	Residence
国籍	Citizenship
私書箱	Post Office Address